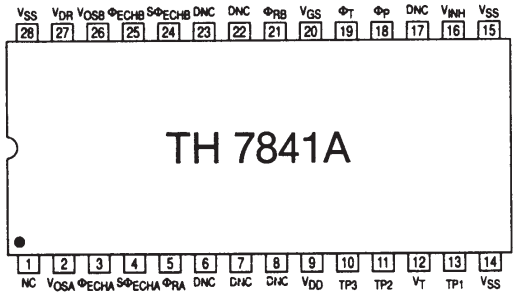
THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

TH7841A

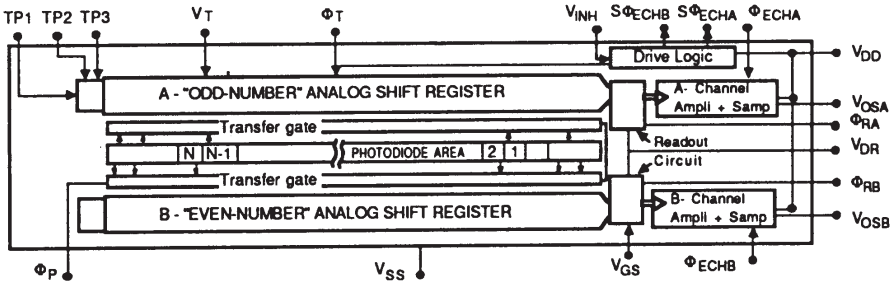
LINEAR CCD* IMAGE SENSOR
2048 PIXELS

- **Pixel size : 11 μm × 13 μm (13 μm pitch).**
- **High data output rate : 20 MHz**
- **High responsivity and resolution over a wide spectral range : from blue (400 nm) up to Near Infrared (1 100 nm).**
- **Low dark signal and improved uniformity.**
- **Low temporal noise and high dynamic range : over 6000/1.**
- **Ease and flexibility of operation :**
  - **Only two external basic drive clocks**
  - **Choice of internal or external sampling and reset.**
- **28-pin DIL package.**
- **Available with standard window or antireflective window in the bandwith 450 to 750 nm.**



PIN IDENTIFICATION

Pin n°	Symbol	Designation
2	V_{OSA}	Video output signal A (odd channel)
3	Φ_{ECHA}	A channel sample-and-hold gate input
4	$S\Phi_{ECHA}$	A channel internal sampling clock output
5	Φ_{RA}	A channel external reset clock input
9	V_{DD}	Output amplifier drain and internal logic supply
10	TP3	Test point 3
11	TP2	Test point 2
12	VT	Register and photosensitive zone DC bias
13	TP1	Test point 1
14, 15, 28	V_{SS}	Substrate bias (Ground)
16	V_{INH}	Internal sampling clock inhibiting input (DC bias)
18	Φ_P	Transfer clock
19	Φ_T	Register transport clock
20	V_{GS}	Output gate DC bias
21	Φ_{RB}	B channel external reset clock input
24	$S\Phi_{ECHB}$	B channel internal sampling clock output
25	Φ_{ECHB}	B channel sample-and-hold gate input
26	V_{OSB}	Video output signal B (even channel)
27	V_{DR}	Reset DC bias
1, 6, 7, 8, 17, 22, 23	DNC	Do not connected



Note : To simplify sensor operation a drive board has been developed and may be purchased from TCS (ref. TH 79K41). This board provides all the necessary electronics : DC supplies, driving clocks and video output buffer.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... – 55°C to + 150°C
Operating temperature ..... 0°C to + 70°C
Thermal cycling ..... 15°C/mn
Maximum voltages :
– Pins : 3, 5, 9, 10, 11, 13, 16, 19, 20, 21, 25, 27 ..... – 0.3 V to + 18 V
– Pins : 12, 18 ..... – 0.3 V to + 16 V
– Pins : 14, 15, 28 ..... 0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Operating range defines the temperature limits between which the functionality is guaranteed : 0°C to 70°C.

OPERATING PRECAUTIONS

Shorting the video output to V_{SS} or V_{DD}, even temporarily, can permanently damage the output amplifier.

OPERATING CONDITIONS (T = 25°C)

Table 1 : DC characteristics

Parameter	Symbol	Values			Unit	Remarks
		Min.	Typ.	Max.		
Output amplifier drain supply	V_{DD}	14	15	16	V	
Reset DC bias	V_{DR}	12	13	14.5	V	Note 1
Output gate DC bias	V_{GS}	5.5	6	6.5	V	
Photosensitive zone and register DC bias	V_T	6	6.5	7	V	Note 2
Substrate bias	V_{SS}	0.0	0.0			
Test point 1	TP1		V_{DD}		V	Note 3
Tests points 2 and 3	TP2, TP3		V_{SS}		V	Note 3

Note 1 : It is recommended to maintain V_{DR} at $V_{DD} - 2$ V.

Note 2 : V_T nominal $= \frac{(V\Phi T) \text{ high} + (V\Phi T) \text{ low}}{2} \pm 5\ \%$.

Note 3 : No use for operation - For testing purpose only.

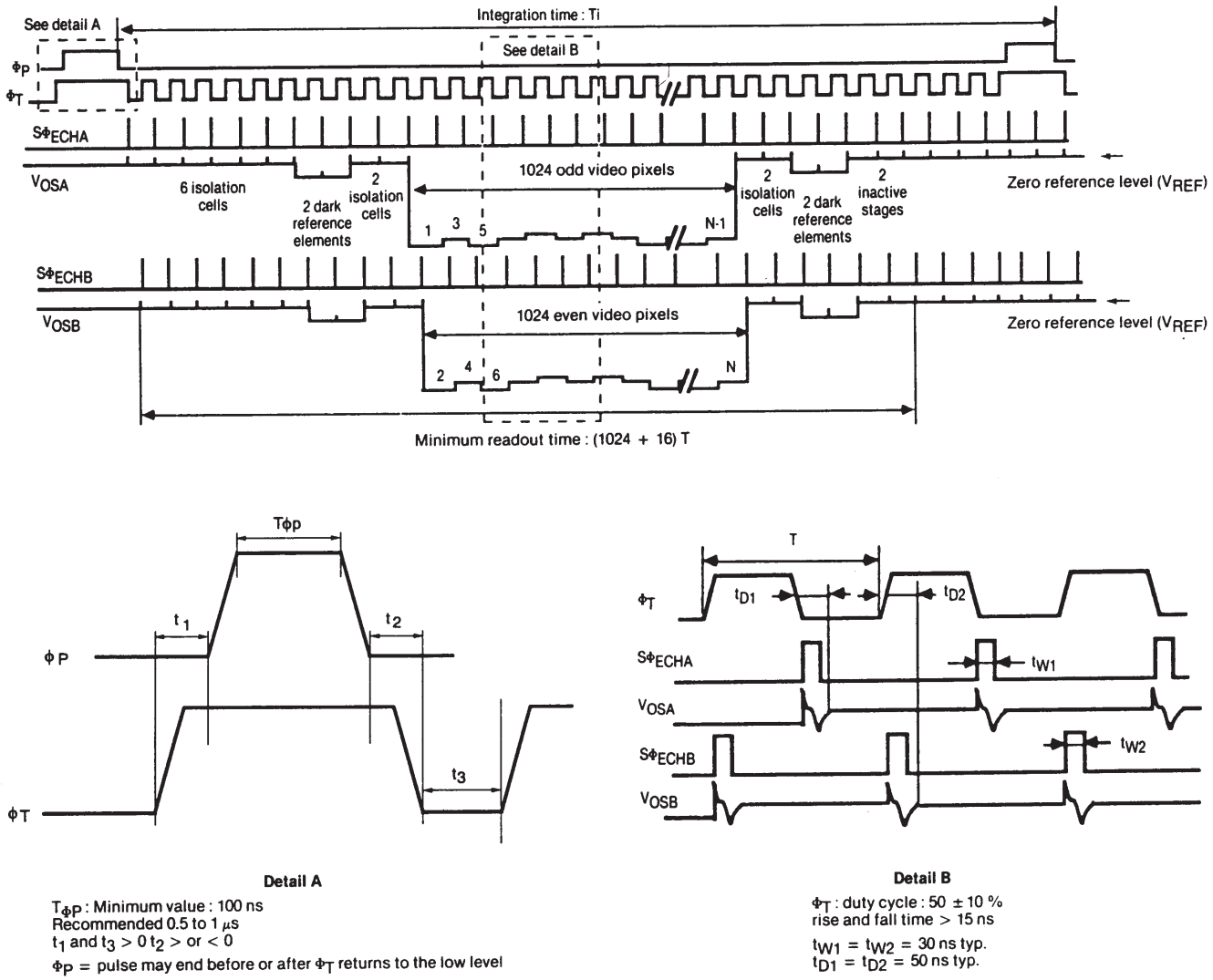
BASIC INTERNAL CONFIGURATION

$S\Phi_{ECHA}$ and Φ_{RA}
$S\Phi_{ECHB}$ and Φ_{RB} internal to TH 7841A

Table 2 : Selection of nominal mode

Option	Implementation	Remarks
Internal sampling	VINH (16) connected to V_{SS} $S\Phi_{ECHA}$ (4) and Φ_{ECHA} (3) strapped $S\Phi_{ECHB}$ (24) and Φ_{ECHB} (25) strapped	see Note
Internal reset	Φ_{RA} (5) and Φ_{RB} (21) connected to VDD	

Note : Make the straps as short as possible to avoid any parasitic coupling to these connections. The load capacitance introduced by the strap should not exceed 5 pF.



Detail A

$T_{\Phi P}$: Minimum value : 100 ns
Recommended 0.5 to 1 µs
t_1 and $t_3 > 0$ $t_2 >$ or < 0
Φ_P = pulse may end before or after Φ_T returns to the low level

Detail B

Φ_T : duty cycle : 50 ± 10 %
rise and fall time > 15 ns
$t_{W1} = t_{W2}$ = 30 ns typ.
$t_{D1} = t_{D2}$ = 50 ns typ.

Figure 1 : Timing diagram
Clocks and video output timing diagram in internal sampling mode.

Table 3 : Drive clock characteristics (see timing diagram - figure 1)

Parameter	Symbol	Logic	Values			Unit	Remarks
			Min.	Typ.	Max.		
Transfer clock Register transport clock	ΦP ΦT	High Low	12 0.0	13 0.4	14 0.6	V	see Note
Register transport clock capacitance	CΦT			800	1200	pF	
Transfer clock capacitance	CΦP			200	300	pF	

Note : Transients under 0.0 V in the clock pulses will lead to charge injection, causing a localized increase in the dark signal. If such spurious negative transients are present, they can be suppressed by inserting a serial resistor of appropriate value (typically 20 to 100 Ω) in the corresponding driver output.

Table 4 : Static and dynamic electrical characteristics

Parameter	Symbol	Values			Unit	Remarks
		Min.	Typ.	Max.		
DC output level	V_{ref}	8	10	12	V	
Output impedance	Z_S		500		Ω	
Register single-stage transfer efficiency	CTE	99.992	99.998		%	V_{OS} = 1 V Note 1
Max. data output frequency	Fs max.	12	20		MHz	Note 2
Input current on pins : 3, 5, 10, 11, 12 13, 18, 19, 20, 21, 25	I_e			2	μA	Ve = 15 V All other pins : 0 V
Peak current sink on Φ_T clock	$(I\Phi T)_P$		500		mA	t_{rise} = 15 ns
Peak current sink on Φ_P clock	$(I\Phi P)_P$		125		mA	t_{rise} = 15 ns
Output amplifier drain supply current	I_{DD}		17		mA	V_{INH} = 0 V V_{DD} = 15 V
Static power dissipation	P_D		155	300	mW	V_{INH} = 0 V V_{DD} = 15 V

Note 1 : V_{OS} = average video output voltage. Measurement excludes first and last pixels.
Note 2 : Fs = $2F\Phi_T$. The minimum clock frequency is limited by the increase in dark signal.

ELECTROOPTICAL PERFORMANCE

General measurement conditions : T_C = 25°C ; T_i = 1 ms ; FΦT = 2.5 MHz.
Light source : tungsten filament lamp (2854 K) + BG 38 filter (2 mm thick) + F/3.5 aperture. The filter limits the spectrum to 700 nm ; in these conditions, 1 μJ/cm² corresponds to 3.5 lux.s.
Typical operating conditions ; internal clock mode (see table 2).
First and last pixels, as well as reference elements, are excluded from the specification.
Measurements taken on each output in succession.

Table 5 : Electrooptical performance

Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Saturation output voltage	V_{SAT}	1.3	1.8	2.2	V	Notes 1 and 2
Saturation exposure	E_{SAT}		0.33		μJ/cm²	
Responsivity	R	2.5	2.9		V/μJ/cm²	
Responsivity unbalance	ΔR/R		2	8	%	Note 3
Photo-response non-uniformity peak-to-peak	PRNU		±5	±10	% V_{OS}	V_{OS} = 50 mV to 1 V
Contrast transfer function at FN (38 l p/mm)	CTF		70		%	V_{OS} ≈ 0.75 V
Temporal noise in darkness			160		μVrms	Note 4
Dynamic range (relative to rms noise)	DR	3000	6000			
Average dark signal	V_{DS}		0.08	0.5	mV	Note 1
Dark signal non-uniformity	DSNU		0.15	0.5	mV	

Note 1 : Value measured with respect to zero reference level (see figure 1).
Note 2 : Conversion factor is typically 1.1 μV/e^-.
Note 3 : ΔR/R is defined as $\frac{200\,|RA-RB|}{RA+RB}$ where { RA is responsivity of video output A ; RB is responsivity of video output B
Note 4 : Measured in Correlated Double Sampling (C.D.S.) mode.

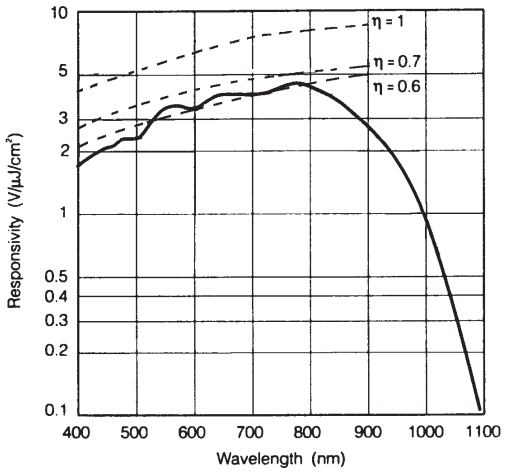


Figure 2 : Typical spectral response.

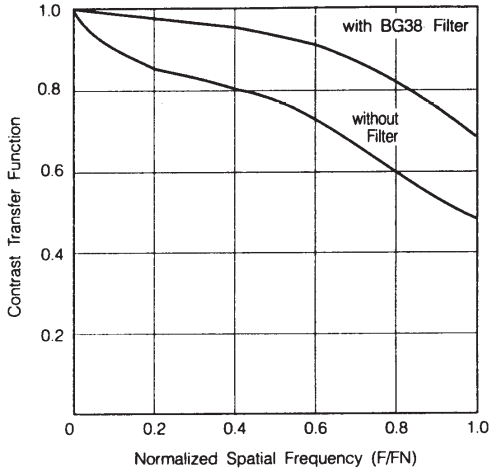


Figure 3 : CTF typical curves (2854 K source).

ELECTROOPTICAL PERFORMANCE WITHOUT INFRARED CUT-OFF FILTERING

The TH 7841A special semiconductor process enables it to exploit the silicon's high near infrared sensitivity while maintaining good imaging performance in terms of response uniformity and resolution. Typical changes in performance with and without IR filtering are summarized below.

	With IR cut-off filter	No IR cut-off filter
Average video signal due to a given scene illumination	V_{OS}	$V_{OS} \times 4$
PRNU (single defects excluded)	± 5 %	± 5 %
CTF at nyquist frequency	70 %	50 %

COMPLEMENTARY OPERATING MODES

TH 7841A may be used in several configurations as regards video output sampling and charge sensing reset.

1) Sampling options

Inhibition of internal sampling pulses allows for two possibilities :

- a) no sampling : video output delivered in unsampled form,
- b) sampling by external clocks : external sampling pulses directly applied to Φ_{ECHA}, Φ_{ECHB} inputs.

If internal sampling clocks $S\Phi_{ECHA}$ and $S\Phi_{ECHB}$ are not used, it is recommended of unpower the corresponding clock drivers, as this will greatly reduce on-chip power consumption.

2) External reset option

The position and period of the charge reset clocks may be optimized by using external clocks on Φ_{RA} and Φ_{RB} inputs. This is specially interesting to optimize the video outputs for Correlated Double Sampling (in order to reduce noise and improve S/N Ratio).

Control signals to be applied in the different configurations are shown in table 6.

Table 6 : Selection of operating modes

Option	Implementation	Remarks
No sampling	Φ_{ECHA} (3) and Φ_{ECHB} (25) connected to VDD $S\Phi_{ECHA}$ (4) and $S\Phi_{ECHB}$ (24) unconnected V_{INH} (16) connected to V_{DD}	see Note
Sampling by external clocks	Sampling clocks connected to Φ_{ECHA}-Φ_{ECHB} $S\Phi_{ECHA}$ and $S\Phi_{ECHB}$ unconnected V_{INH} (16) connected to V_{DD}	See figure 4 for sampling clock timing see Note
Reset control by external clocks	Ext. Φ_{RA} on Φ_{RA} (5) input Ext. Φ_{RB} on Φ_{RB} (21) input	See figure 4 for reset clock timing
Note : Drain supply current I_{DD} decreases from 10 mA to 8 mA typically when internal sampling clock is disabled ($V_{INH} = V_{DD} = 15$ V).		

Table 7 : External Φ_{RA}, Φ_{RB}, Φ_{ECHA}, Φ_{ECHB} clocks characteristics

Parameter	Symbol	Logic	Values			Unit
			Min.	Typ.	Max.	
External reset clock sampling clock	Φ_{RA}, Φ_{RB} Φ_{ECHA}, Φ_{ECHB}	High	12	13	14	V
		Low	0.0	0.4	0.6	V
Reset and sampling clock capacitance	$C\Phi_{RA}$ $C\Phi_{RB}$ $C\Phi_{ECHA}$ $C\Phi_{ECHB}$			10	15	pF

Insertion of a serial resistor (typically 100 Ω) at the driver output avoids spurious negative transients.

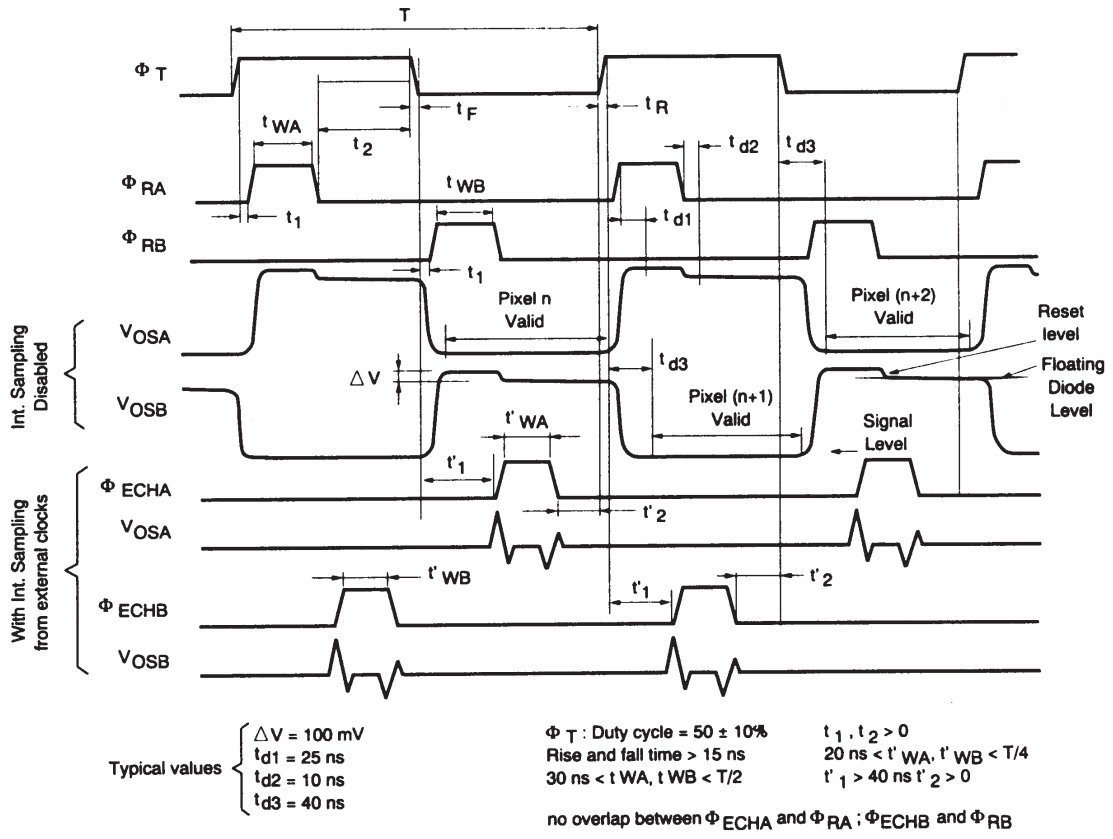


Figure 4 : Timing diagram
Clocks and video output timing diagram with and without on-chip sampling.

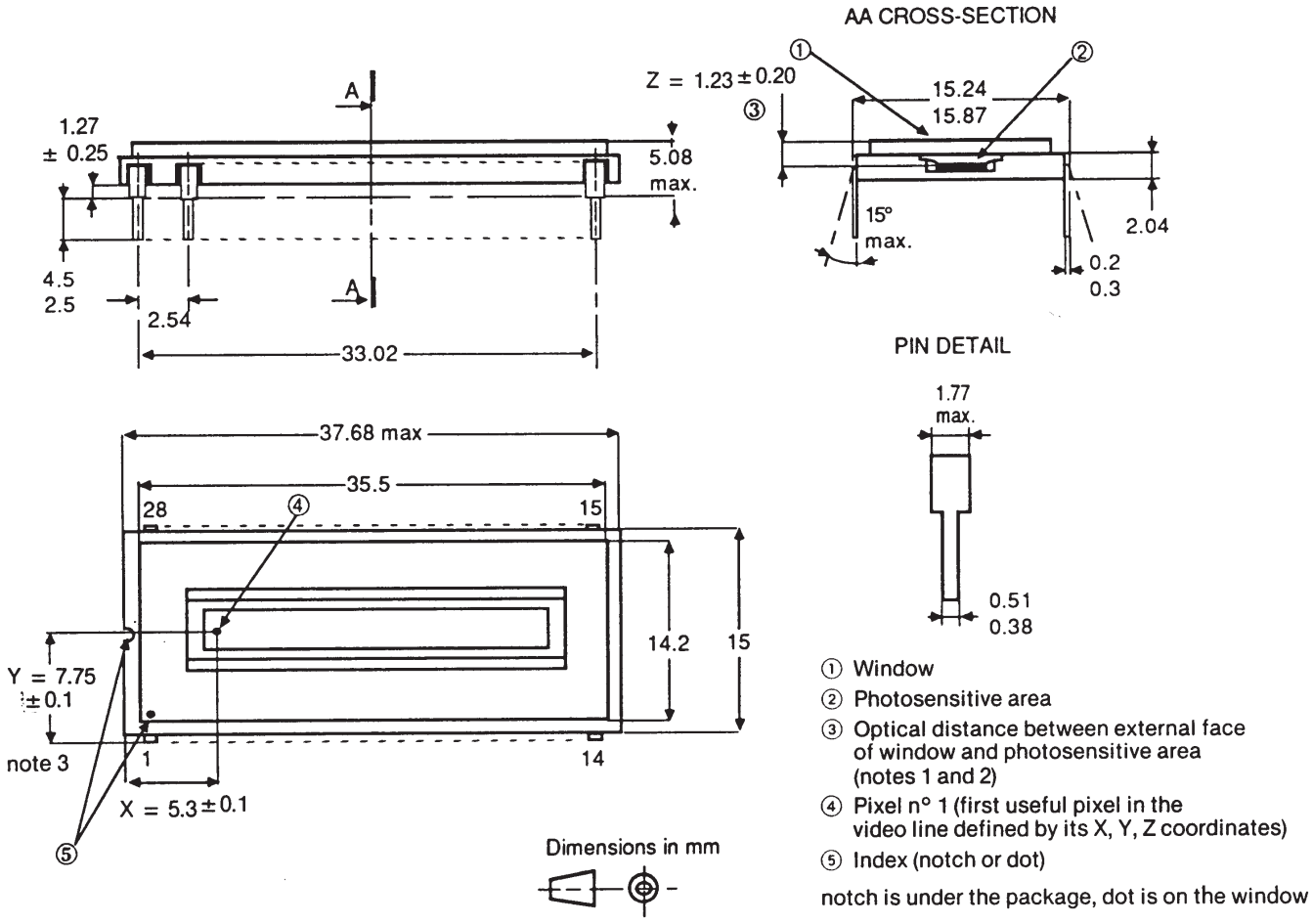
Table 8 : Performances improvement with external Φ_{RA}, Φ_{RB} configuration (see Note)

Parameter	Symbol	Values (Typ.)	Unit
Saturation output voltage	V_{SAT}	2.0	V
Responsivity	R	5.0	V/μJ/cm²
Dynamic range	DR	8 000	

Note 1 : Electrooptical performances obtained with complementary modes are not guaranteed for the standard products.
Note 2 : Conversion factor is typically 1.8 μV/e⁻.

OUTLINE DRAWING

TH 7841A with standard window.



① Window
② Photosensitive area
③ Optical distance between external face of window and photosensitive area (notes 1 and 2)
④ Pixel n° 1 (first useful pixel in the video line defined by its X, Y, Z coordinates)
⑤ Index (notch or dot)

notch is under the package, dot is on the window

Note 1 : If an optical reference is needed, it is recommended to use the window face plane.
Note 2 : Variation of Z (azimuth) on the photosensitive area of a device is ⩽ 0.1 mm.
Note 3 : Variation of Y between the first and the last pixel of the linear area is ⩽ ± 130 μm.

ORDERING CODE

The ordering code is : TH 7841 ACC.

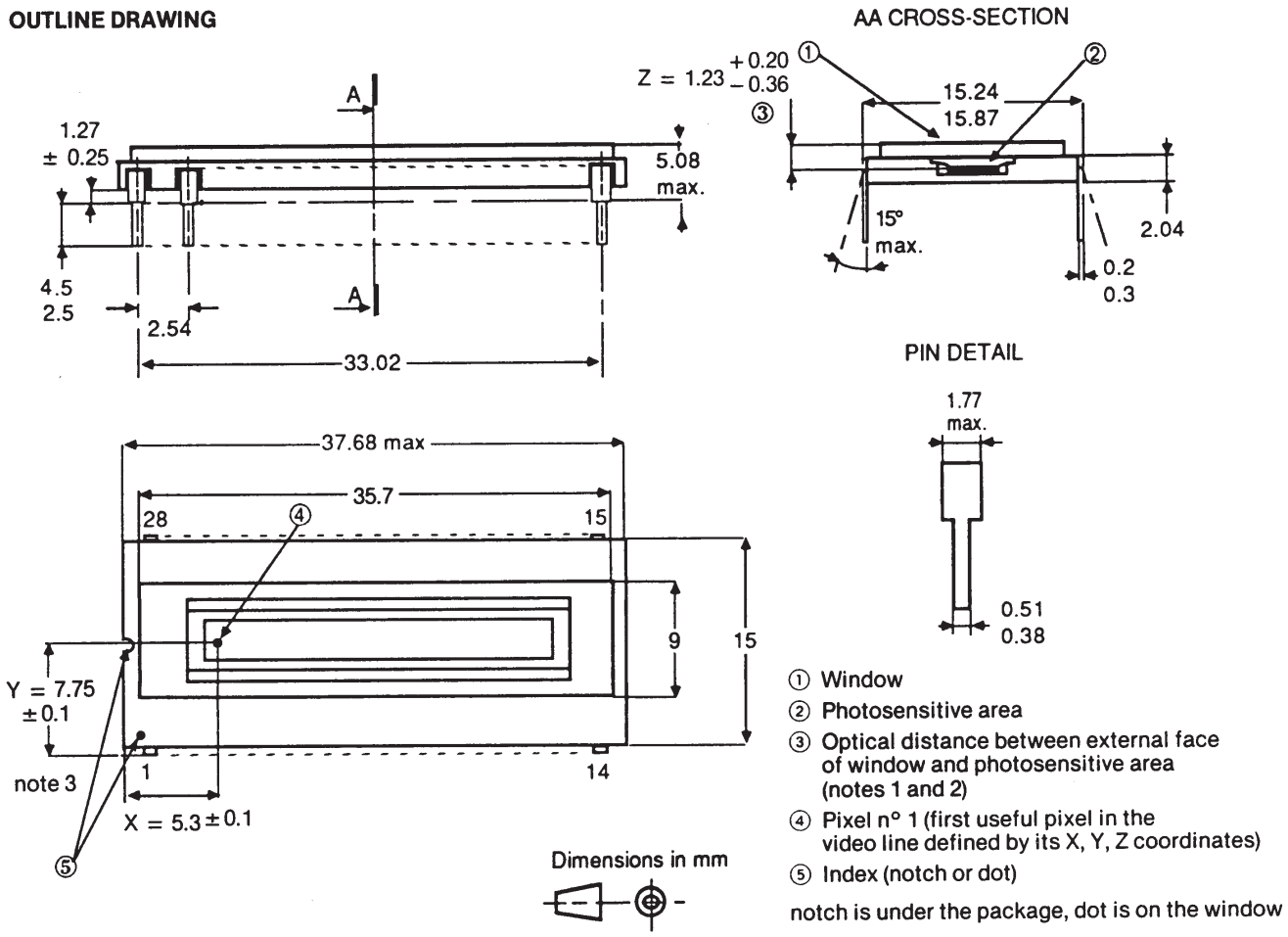
TH 7841A WITH ANTIREFLECTIVE WINDOW

Improvements in the bandwith 450-750 nm :

- 5 % increase in responsitivity (typical value : 3.0 V/μJ/cm²),
- limitation of the parasitic reflections.

Outline drawing.

OUTLINE DRAWING



Note 1 : If an optical reference is needed, it is recommended to use the window face plane.

Note 2 : Variation of Z (azimuth) on the photosensitive area of a device is $\leqslant$ 0.1 mm.

Note 3 : Variation of Y between the first and the last pixel of the linear area is $\leqslant \pm 130\ \mu$m.

ORDERING CODE

The ordering code is : TH 7841 ACC-R.

This product is manufactured by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - 38521 SAINT-EGREVE / FRANCE.

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